|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Bits | Description |
| clk | in | 1 | clock |
| rst | in | 1 | reset |
| filter\_aud\_in\_lft | in | 16 | left parallel digital audio |
| filter\_aud\_in\_rgt | in | 16 | right parallel digital audio |
| filter\_aud\_in\_rts | in | 1 | ready to send |
| filter\_aud\_in\_rtr | out | 1 | read to receive |
| filter\_aud\_out\_lft | out | 16 | left parallel digital audio |
| filter\_aud\_out\_rgt | out | 16 | right parallel digital audio |
| filter\_aud\_out\_rts | out | 1 | ready to send |
| filter\_aud\_out\_rtr | in | 1 | read to receive |
| rf\_filter\_shift | in | 4 | number of bit positions to shift after filter accumulator |
| rf\_filter\_clip\_en | in | 1 | 1- performs clipping 0- no clipping |
| rf\_filter\_coeff[0:255]# | in | 8196 | filter coefficient – 16-bits per coefficient, a total of 512 coefficient |

Filter Block

Interfaces

Functional Requirements

Data Plane Requirements:

* The accumulator precision will be 40 bits and will be shifted by a programmable number of positions (with rounding if right-shifted), clipped, and output as a 16-bit value
* Since the accumulator is 40 bits, there is a low chance for overflow
  + –**Work in Progress**

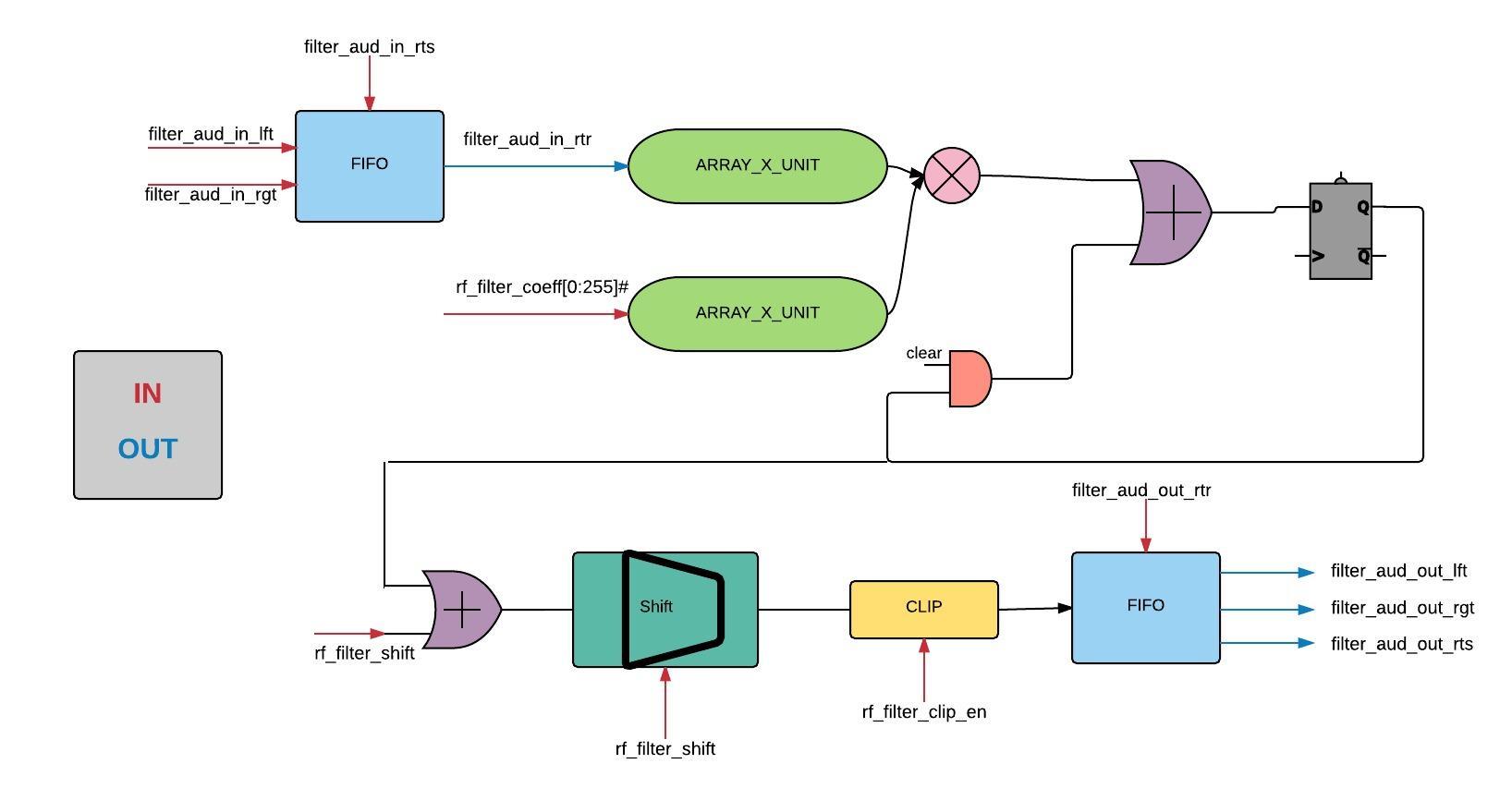
Control Plane Requirements:

* filter\_aud\_in and out interfaces will flow the RTS/RTR protocol outlined in <cite the document>
* Input and output FIFOs may be required to accommodate smooth pipeline flow without bubbles, sizes TBD
* The rf\_\* register values are assumed to be stable. If they change during the calculation of an output sample the result will be unpredictable.

Interfaces Detailed Description:

* RTS/RTR – See <insert reference here>
* Register-based Control
  + rf\_filter\_shift: <what are the permitted values? What do the values mean?>
  + rf\_filter\_clip\_en: 1 – clipping will be performed, 0 – wrapping will be performed on overflow
  + rf\_filter\_coeff\_###: <insert description>
* Status Bits:
  + <maybe indicate FIFO overflow/underflow? If so then need a “trig” register signal to clear the bits>
  + <maybe indicate clipping/wrapping? If so need trig signal to clear>

Micro-architecture



filter\_convolution.v

filter\_accumulator.v

filter\_fifo.v

filter\_round\_shift\_clip.v

Design

Verification